DERWENT-ACC-NO: 1998-568993

DERWENT-WEEK: 200313

TITLE: Semiconductor integrated circuit - includes microprogram-controlled control and processing sections which form test patterns of memory in accordance with prescribed algorithm

INVENTOR: FUKIAGE, H; SATOH, M ; SHIMIZU, I ; SATOU, M

PATENT-ASSIGNEE: HITACHI LTD[HITA]

PRIORITY-DATA: 1997JP-0326279 (November 27, 1997) , 1997JP-0098840 (April 16, 1997)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
WO 9847152 A1	October 22, 1998	J	056	G11C 029/00
JP 10543742 X	October 3, 2000	N/A	000	G11C 029/00
US 6233182 B1	May 15, 2001	N/A	000	G11C 007/00
KR 2001006400 A	January 26, 2001	N/A	000	G11C 029/00
US 6467056 B1	October 15, 2002	N/A	000	G11C 029/00

DESIGNATED-STATES: CN JP KR SG US AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
WO 9847152A1	N/A	1998WO-JP01731	April 16, 1998
JP 10543742X	N/A	1998JP-0543742	April 16, 1998
JP 10543742X	N/A	1998WO-JP01731	April 16, 1998
JP 10543742X	Based on	WO 9847152	N/A
US 6233182B1	N/A	1998WO-JP01731	April 16, 1998
US 6233182B1	N/A	1999US-0403104	December 15, 1999
US 6233182B1	Based on	WO 9847152	N/A
KR2001006400A	N/A	1999KR-0709487	October 15, 1999
US 6467056B1	Div ex	1998WO-JP01731	April 16, 1998
US 6467056B1	Div ex	1999US-0403104	December 15, 1999
US 6467056B1	N/A	1999US-0461401	December 15, 1999
US 6467056B1	Div ex	US 6233182	N/A

INT-CL (IPC): G01R031/28, G11C007/00 , G11C029/00

ABSTRACTED-PUB-NO: US 6233182B

BASIC-ABSTRACT:

A test circuit composed of microprogram-controlled control and processing sections which form test patterns (address and data) of a memory in accordance with a prescribed algorithm and, at the same time, read out written data, and a data discriminating member which discriminates the read-out data and outputs discriminated results is provided on a semiconductor chip on which the memory is mounted.

ABSTRACTED-PUB-NO: US 6467056B

EQUIVALENT-ABSTRACTS:

A test circuit composed of microprogram-controlled control and processing sections which form test patterns (address and data) of a memory in accordance with a prescribed algorithm and, at the same time, read out written data, and a data discriminating member which discriminates the read-out data and outputs discriminated results is provided on a semiconductor chip on which the memory is mounted.

A test circuit composed of microprogram-controlled control and processing sections which form test patterns (address and data) of a memory in accordance with a prescribed algorithm and, at the same time, read out written data, and a data discriminating member which discriminates the read-out data and outputs discriminated results is provided on a semiconductor chip on which the memory is mounted.

WO 9847152A

CHOSEN-DRAWING: Dwg.1/12

TITLE-TERMS: SEMICONDUCTOR INTEGRATE CIRCUIT MICROPROGRAM CONTROL CONTROL
PROCESS SECTION FORM TEST PATTERN MEMORY ACCORD PRESCRIBED ALGORITHM

DERWENT-CLASS: S01 T01 U11 U13 U14

EPI-CODES: S01-G01; T01-G02A2A; U11-F01C3; U11-F01D2; U13-C07; U14-D01B;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1998-442659

DERWENT-ACC-NO: 2001-060362

DERWENT-WEEK: 200242

TITLE: Semiconductor integrated circuit and method for designing logic integrated circuit comprising the same

INVENTOR: OSHIMA, T;-SATOH, M ; SHIMIZU, I ; TAKAHASHI, H

PATENT-ASSIGNEE: HITACHI LTD[HITA]

PRIORITY-DATA: 1999WO-JP01035 (March 4, 1999)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
WO 200052753 A1	September 8, 2000	J	000	H01L 021/82
JP 2000603090 X	June 18, 2002	N/A	000	H01L 021/82

DESIGNATED-STATES: JP KR US AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
WO 200052753A1	N/A	1999WO-JP01035	March 4, 1999
JP2000603090X	N/A	1999WO-JP01035	March 4, 1999
JP2000603090X	N/A	2000JP-0603090	March 4, 1999
JP2000603090X	Based on	WO 200052753	N/A

INT-CL (IPC): G06F017/50, H01L021/82 , H01L021/822 , H01L027/04

ABSTRACTED-PUB-NO: WO200052753A

BASIC-ABSTRACT:

NOVELTY - By using a semiconductor integrated self-constituting circuit capable of constituting an arbitrary logic, a control unit or control circuit interprets design data of function level described in a language, for example, HDL, and a signal for determining the logic structure of the self-constituting circuit is fed from the control unit or control circuit to the self-constituting circuit so as to constitute a logic integrated circuit having a desired logic function.

USE - None given.

CHOSEN-DRAWING: Dwg.0/0

TITLE-TERMS: SEMICONDUCTOR INTEGRATE CIRCUIT METHOD DESIGN LOGIC INTEGRATE CIRCUIT COMPRISE

DERWENT-CLASS: T01 U11 U13

EPI-CODES: T01-J15A1; T01-S01B; U11-G; U13-C04D;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N2001-045160